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EXAMINER	
STIGLIC, RYAN M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	**Application No.** 10/683,859	**Applicant(s)** KELLEY ET AL.
	Examiner Ryan M. Stiglic	**Art Unit** 2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/30/06*.
2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-32* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-32 are pending and have been examined.

2. Claims 1-32 are rejected.

Response to Amendment

3. The declaration filed on January 30, 2006 under 37 CFR 1.131 has been considered but is ineffective to overcome the Barker reference.

The evidence submitted is insufficient to establish a conception of the invention prior to the effective date of the Barker reference. While conception is the mental part of the inventive act, it must be capable of proof, such as by demonstrative evidence or by a complete disclosure to another. Conception is more than a vague idea of how to solve a problem. The requisite means themselves and their interaction must also be comprehended. See *Mergenthaler v. Scudder*, 1897 C.D. 724, 81 O.G. 1417 (D.C. Cir. 1897).

Rule 37 CFR 1.131(b) provides three ways in which an applicant can establish prior invention of the claimed subject matter. The showing of facts must be sufficient to show:

> a. (actual)< reduction to practice of the invention prior to the effective date of the reference; or
> b. conception of the invention prior to the effective date of the reference coupled with due diligence from prior to the reference date to a subsequent (actual) reduction to practice; or
> c. conception of the invention prior to the effective date of the reference coupled with due diligence from prior to the reference date to the filing date of the application (constructive reduction to practice).

See MPEP § 715.07 III

Insofar as applicant has not alleged nor disclosed an Actual Reduction to Practice the Examiner understands applicant has attempted to show prior invention through option (c), conception coupled with due diligence. The Examiner understands Exhibit A, dated May 16, 2003, to be applicant's evidence of conception (as supported by statements 3 and 4 of the declaration of Paul J. Polansky). An affidavit or declaration under 37 CFR 1.131 "must establish possession of either the whole invention claimed or something falling within the claim, in the sense that the claim as a whole reads on it (*see MPEP § 715.02*)." Moreover, "The facts to be established under 37 CFR 1.131 are similar to those to be provided in interference (*see MPEP §715.07 III*)." See also Coleman v. Dines, 754 F.2d 353, 224 USPQ 857 (Fed. Cir. 1985) (It is settled that in establishing conception a party must show possession of every feature recited in the count, and that every limitation of the count must have been known to the inventor at the time of the alleged conception. Conception must be proved by corroborating evidence.) *see MPEP § 2138.04*. In summary conception is successfully established when applicant has clearly demonstrated how each and every limitation of the claims in question have been disclosed in the evidence (i.e. a clear mapping). Furthermore, it is noted that the invention disclosure form dated May 16, 2003 states, "Please attach copy of first drawing(s) of the intention, with date(s)" and in response to this requirement applicant's noted, "Done on the whiteboard in Brantley's cube on 2003 May 12th (page 3 of Exhibit A)." "Evidence in the form of exhibits may accompany the affidavit or declaration...For example, the allegations of fact might be supported by submitting as evidence one or more of the following: (A) attached sketches; (B) attached blueprints; (C) attached photographs (etc...) (*see MPEP § 715.07*)"

With respect to due diligence Exhibit B, dated July 29, 2003, and Exhibit C, dated August 13, 2003, have been submitted in an attempt to show diligence from the time period just prior to June 24, 2003 up until the filing of the instant application on October 10, 2003. "In determining the sufficiency of a 37 CFR 1.131 affidavit or declaration, diligence need not be considered unless conception of the invention prior to the effective date is clearly established, since diligence comes into question only after prior conception is established. Ex parte Kantor, 177 USPQ 455 (Bd. App. 1958) (*see MPEP § 715.07(a)*)." Despite the lack of a clearly established conception the Examiner will address the allegation of diligence in an effort to advance prosecution. "What is meant by diligence is brought out in Christie v. Seybold, 1893 C.D. 515, 64 O.G. 1650 (6th Cir. 1893). In patent law, an inventor is either diligent at a given time or he is not diligent; there are no degrees of diligence. An applicant may be diligent within the meaning of the patent law when he or she is doing nothing, if his or her lack of activity is excused. Note, however, that the record must set forth an explanation or excuse for the inactivity; the USPTO or courts will not speculate on possible explanations for delay or inactivity. See In re Nelson, 420 F.2d 1079, 164 USPQ 458 (CCPA 1970). Diligence must be judged on the basis of the particular facts in each case. See MPEP § 2138.06 for a detailed discussion of the diligence requirement for proving prior invention (*cited from MPEP § 715.07(a)*)."

"An applicant must account for the entire period during which diligence is required. Gould v. Schawlow, 363 F.2d 908, 919, 150 USPQ 634, 643 (CCPA 1966) (Merely stating that there were no weeks or months that the invention was not worked on is not enough.); In re Harry, 333 F.2d 920, 923, 142 USPQ 164, 166 (CCPA 1964) (statement that the subject matter "was diligently reduced to practice" is not a showing but a mere pleading). A 2-day period lacking activity has been held to be fatal. In re Mulder, 716 F.2d 1542, 1545, 219 USPQ 189, 193 (Fed. Cir. 1983) (37 CFR 1.131 issue); Fitzgerald v. Arbib, 268 F.2d 763, 766, 122 USPQ 530, 532 (CCPA 1959) (Less than 1 month of inactivity during critical period. Efforts to exploit an invention commercially do not constitute diligence in reducing it to practice. An actual reduction to practice in the case of a design for a three-dimensional article requires that it should be embodied in some structure other than a mere drawing.); Kendall v. Searles, 173 F.2d 986, 993, 81 USPQ 363, 369 (CCPA 1949) (Diligence requires that applicants must be specific as to dates and facts.). "The period during which diligence is required must be accounted for by either affirmative acts or acceptable excuses. Rebstock v. Flouret, 191 USPQ 342, 345 (Bd. Pat. Inter. 1975) (*cited from MPEP § 2138.06*)." "The diligence of attorney in preparing and filing patent application inures to the benefit of the inventor. Conception was established at least as early as the date a draft of a patent application was finished by a patent attorney on behalf of the inventor. Conception is less a matter of signature than it is one of disclosure. Attorney does not prepare a patent application on behalf of particular named persons, but on behalf of the true inventive entity. Six days to execute and file application is acceptable. Haskell v. Coleburne, 671 F.2d 1362, 213 USPQ 192, 195 (CCPA 1982). See also Bey v. Kollonitsch, 866 F.2d 1024, 231 USPQ 967 (Fed. Cir. 1986) (Reasonable diligence is all that is required of the attorney.

Reasonable diligence is established if attorney worked reasonably hard on the application during the continuous critical period. If the attorney has a reasonable backlog of unrelated cases which he takes up in chronological order and carries out expeditiously, that is sufficient. Work on a related case(s) that contributed substantially to the ultimate preparation of an application can be credited as diligence.) (*cited from MPEP § 2138.06*)". In summary applicant has failed to show due diligence for the *entire* time period from just prior to June 24, 2003 (the filing of Barker) to the filing of the instant application (October 10, 2003). The applicant has failed to provide evidence of diligence, or reasonable excuses, for the time period from just prior to the filing of Barker (June 24, 2003) to the reception of the letter marked Exhibit B (received July 29, 2003). The applicant has also failed to provide evidence of diligence, or reasonable excuses, for the time period between the receptions of the letter marked Exhibit B (received July 29, 2003) to the subject matter conflict of interest check marked Exhibit C (dated August 13, 2003). Finally, the applicant has failed to provide evidence of diligence, or reasonable excuses, for the time period between the subject matter conflict of interest check marked Exhibit C (dated August 13, 2003) to the filing of the instant application on October 10, 2003.

Response to Arguments

4. Applicant's arguments, regarding claims 12 and 20-22 as being non-obvious under 35 U.S.C. § 103(a), filed January 30, 2006 have been fully considered but they are not persuasive. Barker teaches [0026] that the processor surrogate is implemented as an integrated circuit package. Moreover, Homer teaches the switchable circuit component is integrated onto a single component (col. 4, ll. 51-65).

5. Applicant's arguments, see page 10, filed January 30, 2006, with respect to the rejection(s) of claim(s) 1, 4-6, 9, 12-16, 19-20, 23-24 and 27-32 under 35 U.S.C. § 103(a) have been fully considered and are persuasive. Kessler does not disclose a computer system comprising a processor surrogate "characterized as not having its own central processing unit." Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Barker et al.

Information Disclosure Statement

6. The information disclosure statement filed December 29, 2005 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. The cited US Patents have been reviewed and considered however there exists no copy of the Cost Journal article titled "Swift Interconnects Ripple the Multiprocessing Waters" as disclosed on the IDS Citation Number 1-A. As such the Non-patent Literature Citation Number 1-A has not been considered.

Claim Rejections - 35 USC § 102

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 1-3 and 9-11 rejected under 35 U.S.C. 102(e) as being anticipated by Barker et al (US 20040268000A1).

For claim 1 Barker discloses:

A processor surrogate for use in a processing node of a multiprocessor data processing system having a plurality of processing nodes coupled together and to a plurality of input/output devices using corresponding communication links, the processor surrogate comprising:

- a first port comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link for coupling to one of the plurality of processing nodes (Fig. 3 and 4, item 202; [0025-0026]);
- a second port comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link for coupling to one of the plurality of input/output devices (Fig. 3 and 4, item 202; [0025-0026]); and
- an interconnection circuit coupled between said first port and said second port (Fig. 4 depicts "wiring that connects two of the point-to-point links"; [0025-0026]);
- wherein the processor surrogate is characterized as not having its own central processing unit (Fig. 4, 202; [0026-0027]).

For claim 2 Barker discloses:

The processor surrogate of claim 1 wherein said interconnection circuit comprises a passive interconnection between said first port and said second port (Fig. 4; [0025-0026]).

For claim 3 Barker discloses:

The processor surrogate of claim 2 wherein said interconnection circuit further comprises:

- a first set of internal connections between a plurality of input terminals of said first port and a corresponding plurality of output terminals of said second port (Fig. 4; [0025-0026]); and
- a second set of internal connections between a plurality of input terminals of said second port and a corresponding plurality of output terminals of said first port (Fig. 4; [0025-0026]).

For claim 9 Barker discloses:

A processor surrogate for use in a multiprocessor data processing system having a first processing node including an actual processor and a second processing node coupled to the first processing node and including the processor surrogate, the processor surrogate comprising:

- an integrated circuit package having a first plurality of terminals forming a first port of the processor surrogate and disposed at locations corresponding to a first link controller of the actual processor, and a second plurality of terminals forming a second port of the processor surrogate and disposed at locations corresponding to a second link controller of the actual processor (Fig. 4; [0025-0026]); and
- a plurality of electrical connections between said first plurality of terminals of said first port and corresponding ones of said second plurality of terminals of said second port (Fig. 4; [0025-0026]);

- wherein the processor surrogate is characterized as not having its own central processing unit (Fig. 4, 202; [0026-0027]).

For claim 10 Barker discloses:

The processor surrogate of claim 9 wherein said plurality of electrical connections comprises:

- a first set of internal connections between a plurality of input terminals of said first port and a corresponding plurality of output terminals of said second port (Fig. 4; [0025-0026]); and
- a second set of internal connections between a plurality of input terminals of said second port and a corresponding plurality of output terminals of said first port (Fig. 4; [0025-0026]).

For claim 11 Barker discloses:

The processor surrogate of claim 9 wherein said first and second link controllers of the actual processor are substantially compatible with the HyperTransport. I/O Link Specification, Revision 1.05 [0023,0026].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 12 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barker et al. as applied to claim 9 above, and further in view of Homer et al. (US006626690B2).

Barker discloses a passive surrogate processor that allows communications to pass-through the surrogate processor directly to another connected device. In other words the surrogate processor of Barker discloses directly connecting the pins on an input side the surrogate processor to the output pins on the surrogate processor such that all signals presented to the surrogate processor on the input side are forwarded to the output side [0025-0026]. Barker discloses that when a surrogate processor is placed in a multiprocessor system two processors that were once two 'hops' away are now one 'hop' away since the surrogate processor does not consume the signals presented to it from either neighbor processor. Barker however fails to disclose directly connecting an actual processor to the memory/I/O of the surrogate processor (once actual processor).

Homer teaches a low profile jumper solution for selectively connecting various system components (Fig. 1-5). The low profile jumper solution (hereinafter multi-directional connector) is usable as a removable module of a computer system wherein system components are selectively coupled according to the orientation o the multi-directional connector (col. 5, line 22 – col. 6, line 27). The multi-directional connector of Homer allows various system devices (such as processors, memory, or I/O) to be selectively coupled to other system devices while isolating remaining system devices (col. 2, ll. 16-21; col. 2, ll. 36-38; col. 4, ll. 2-5).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the multi-directional connector of Homer into the surrogate processor of Barker thus facilitating multiple switchable connections in a relatively low profile connector assembly.

For claim 12:

The processor surrogate of claim 9 wherein the multiprocessor data processing system further comprises an input/output device coupled to said second port of the processor surrogate (The invention of Barker in view of Homer provides a user with the ability to selectively connect processors to either one another or to the I/O/memory of the replaced processor by simply changing the orientation of the surrogate processor).

For claim 20:

A multiprocessor data processing system comprising:

- a first processing node comprising an actual processor (Barker; Fig. 3, 102; [0025-0026]);
- a second processing node comprising a processor surrogate having an integrated circuit package and (Barker; Fig. 4, 202; [0026-0027]) a first port coupled to said first processing node, a second port, and an interconnection circuit coupled between said first port and said second port (Barker; Fig. 3 & 4, 202; [0025-0026]), wherein the processor

surrogate is characterized as not having its own central processing unit (Barker; Fig. 4, 202; [0026-0027]).; and

- an input/output device coupled to said second port of said second processing node and accessible to said actual processor via said processor surrogate (The invention of Barker in view of Homer provides a user with the ability to selectively connect processors to either one another or to the I/O/memory of the replaced processor by simply changing the orientation of the surrogate processor).

For claim 21:

The multiprocessor data processing system of claim 20 wherein said interconnection circuit comprises a passive interconnection between said first port and said second port (Barker; [0025-0026]).

For claim 22:

The multiprocessor data processing system of claim 21 wherein said interconnection circuit further comprises:

- a first set of internal connections between a plurality of input terminals of said first port and a corresponding plurality of output terminals of said second port (Barker; Fig. 4; [0025-0026]); and
- a second set of internal connections between a plurality of input terminals of said second port and a corresponding plurality of output terminals of said first port (Barker; Fig. 4; [0025-0026]).

11. Claims 1, 4-6, 9, 12-16, 19-20, 23-24, 27-32 rejected under 35 U.S.C. 103(a) as being unpatentable over Kessler et al. (US006633960B1) in view of Barker et al. (US 20040268000A1).

For claim 1 Kessler in view of Barker teach:

A processor surrogate (pass-through processor; col. 5, ll. 29-40) for use in a processing node of a multiprocessor data processing system having a plurality of processing nodes coupled together and to a plurality of input/output devices using corresponding communication links, the processor surrogate comprising:

- a first port comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link for coupling to one of the plurality of processing nodes (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200);
- a second port comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link for coupling to one of the plurality of input/output devices (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]); and
- an interconnection circuit coupled between said first port and said second port (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals).

Kessler teaches a multiprocessor system comprising a plurality of processing nodes **100**. Each processing node comprises a N, S, E, and W port for communicating with an adjacent processor (Fig. 1 and 2; col. 4, line 60 – col. 5, line 14). Furthermore, each processing node possesses a port for I/O communications (col. 5, ll. 15-20) and a port for memory communications (col. 5, ll. 21-28). Kessler goes on to teach, if a physical connection is not present between a pair of processors (i.e. a processor is missing or has been removed), a bypass path is implemented using a pass-through in each processor (col. 5, ll. 29-40). A pass-through in each processor permits each processor to access a pass-through processor's (a missing processor's) memory and I/O devices (col. 5, ll. 38-39). Kessler does not expressly teach the composition of a pass-through processor however Kessler does provide one potential solution in inter-processor and I/O router unit **200** ("RBOX", col. 5, ll. 41-50). The RBOX **200** provides interfaces to as many as four other processors, an I/O controller and memory (Fig. 2b; col. 12, ll. 11-15). Therefore Kessler teaches the presence of the RBOX in a pass-through of each processor since the pass-through of each processor permits access to a processor's memory and I/O devices (col. 5, ll. 35-40). While Kessler teaches a pass-through or bypass path is provided in each processor in case physical connections are not present between each pair of processors, Kessler does not expressly teach the pass-through or bypass path is implemented in a separate surrogate processor characterized as not having its now central processing unit.

Barker teaches a processor surrogate for use in a processing node of a multiprocessor data processing system having a plurality of processing nodes coupled together and to a plurality of input/output devices using corresponding communication links, the processor surrogate comprising:

- a first port comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link for coupling to one of the plurality of processing nodes (Fig. 3 and 4, item 202; [0025-0026]);
- a second port comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link for coupling to one of the plurality of input/output devices (Fig. 3 and 4, item 202; [0025-0026]); and
- an interconnection circuit coupled between said first port and said second port (Fig. 4 depicts "wiring that connects two of the point-to-point links"; [0025-0026]);
- wherein the processor surrogate is characterized as not having its own central processing unit (Fig. 4, 202; [0026-0027]).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the processor surrogate of Barker into the computer system of Kessler in order to improve system symmetry and reduce overall latency thereby potentially improving performance of the computer system (Barker; 0007]). Therefore, by replacing a processor of Kessler where "physical connections are not present between each pair of processors" with a processor surrogate of Barker overall latency is reduced thereby improving system performance.

For claim 4 Kessler in view of Barker teach:

The processor surrogate of claim 1 wherein said interconnection circuit comprises an active interconnection between said first port and said second port (Fig. 2b, RBOX **200;** col. 12, ll. 11-15).

For claim 5 Kessler in view of Barker teach:

The processor surrogate of claim 4 wherein said interconnection circuit further comprises:

- a first communication link controller coupled to said first port (Fig. 2b, boxes N, S, E, W attached to router/RBOX **200**);
- a second communication link controller coupled to said second port (Fig. 2b, the box labeled IO connected to router/RBOX **200**; see also Fig. 1, 104); and
- a crossbar switch having a first terminal coupled to said first communication link controller, and a second terminal coupled to said second communication link controller (Router/RBOX **200** acts as a crossbar switch forwarding communication signals from one port to another).

For claim 6 Kessler in view of Barker teach:

The processor surrogate of claim 5 wherein said interconnection circuit further comprises:

- a memory controller coupled to said crossbar switch and adapted to be coupled to an external memory, for controlling accesses between said first and second communication link controllers and said external memory (Fig. 2b, 190; col. 5, ll. 47-50; col. 11, ll. 50-52).

For claim 9 Kessler in view of Barker teach:

A processor surrogate for use in a multiprocessor data processing system having a first processing node including an actual processor and a second processing node coupled to the first processing node and including the processor surrogate, the processor surrogate comprising:

- an integrated circuit package having a first plurality of terminals forming a first port of the processor surrogate and disposed at locations corresponding to a first link controller of the actual processor, and a second plurality of terminals forming a second port of the processor surrogate and disposed at locations corresponding to a second link controller of the actual processor (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W] and contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]. Figure 2b shows the four ports connected to router [RBOX] 200); and
- a plurality of electrical connections between said first plurality of terminals of said first port and corresponding ones of said second plurality of terminals of said second port (the RBOX **200** serves as the electrical connections between the various ports).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler and Barker.

For claim 12 Kessler in view of Barker teach:

The processor surrogate of claim 9 wherein the multiprocessor data processing system further comprises an input/output device coupled to said second port of the processor surrogate (Fig. 1

and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]).

For claim 13 Kessler in view of Barker teach:

A processor surrogate for use in a multiprocessor data processing system having a plurality of processing nodes comprising a first processing node including an actual processor and a second processing node coupled to the first processing node and including the processor surrogate, the processor surrogate comprising:

- a first port comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link and thereby to one of the plurality of processing nodes (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200);
- a second port comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link and thereby to an input/output device (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]); and
- an active interconnection circuit coupled between said first port and said second port to thereby couple said one of the plurality of processing nodes and said input/output device (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals);

- wherein the processor surrogate is characterized as not having its own central processing unit (Barker; Fig. 4, 202; [0026-0027]).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler and Barker.

For claim 14 Kessler in view of Barker teach:

The processor surrogate of claim 13 wherein said one of the plurality of processing nodes comprises said first node including said actual processor (As previously discussed, Kessler teaches a surrogate processor (also known as a pass-through processor), is inserted into the multiprocessor system to allow actual processors to access the memory and I/O device of a processor that has been removed).

For claim 15 Kessler in view of Barker teach:

The processor surrogate of claim 13 wherein said active interconnection circuit comprises:

- a first communication link controller coupled to said first port (Fig. 2b, boxes N, S, E, W attached to router/RBOX **200**);
- a second communication link controller coupled to said second port (Fig. 2b, the box labeled IO connected to router/RBOX **200**; see also Fig. 1, 104); and
- a crossbar switch having a first terminal coupled to said first communication link controller, and a second terminal coupled to said second communication link controller

(Router/RBOX **200** acts as a crossbar switch forwarding communication signals from one port to another).

For claim 16 Kessler in view of Barker teach:

The processor surrogate of claim 15 further comprising: a memory controller coupled to said crossbar switch and adapted to be coupled to an external memory, for controlling accesses between said first and second communication link controllers and said external memory (Fig. 2b, 190; col. 5, ll. 47-50; col. 11, ll. 50-52).

For claim 19 Kessler in view of Barker teach:

The processor surrogate of claim 13 further comprising:

- a third port comprising a third set of integrated circuit terminals coupled to said active interconnection circuit and adapted to be coupled to a third external communication link and thereby to a second input/output device (Kessler teaches an I/O port of the processor surrogate connects to a plurality of I/O devices **105 and 106**. While Kessler may only expressly teach the use of one I/O port connected to the RBOX, one of ordinary skill in the art would be able to easily modify the invention of Kessler such that an additional I/O port is added to provide additional I/O devices, thus increasing the connectivity of the multiprocessor system).

For claim 20 Kessler in view of Barker teach:

A multiprocessor data processing system (Fig. 1, 90) comprising:

- a first processing node comprising an actual processor (Fig. 1, 100);
- a second processing node comprising a processor surrogate (pass-through processor; col. 5, ll. 29-40) having a first port coupled to said first processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), a second port (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]), and an interconnection circuit coupled between said first port and said second port (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals); and
- an input/output device coupled to said second port of said second processing node and accessible to said actual processor via said processor surrogate (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals to the I/O controller **104** and I/O devices **105 and 106**).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler.

For claim 23 Kessler in view of Barker teach:

The multiprocessor data processing system of claim 20 wherein said interconnection circuit comprises an active interconnection between said first port and said second port (Fig. 2b, RBOX **200;** col. 12, ll. 11-15).

For claim 24 Kessler in view of Barker teach:

The multiprocessor data processing system of claim 23 wherein said interconnection circuit further comprises:

- a first communication link controller coupled to said first port (Fig. 2b, boxes N, S, E, W attached to router/RBOX **200**);
- a second communication link controller coupled to said second port (Fig. 2b, the box labeled IO connected to router/RBOX **200**; see also Fig. 1, 104); and
- a crossbar switch having a first terminal coupled to said first communication link controller, and a second terminal coupled to said second communication link controller (Router/RBOX **200** acts as a crossbar switch forwarding communication signals from one port to another).

For claim 27 Kessler in view of Barker teach:

The multiprocessor data processing system of claim 24 further comprising:

- a memory controller coupled to said crossbar switch and adapted to be coupled to an external memory, for controlling accesses between said first and second communication link controllers and said external memory (Fig. 2b, 190; col. 5, ll. 47-50; col. 11, ll. 50-52).

For claim 28 Kessler in view of Barker teach:

A multiprocessor data processing system comprising:

- a first processing node comprising an actual processor (Fig. 1, 100);
- a second processing node comprising a first processor surrogate (pass-through processor; col. 5, ll. 29-40) having a first port coupled to said first processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), a second port (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]), a third port (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), and an interconnection circuit coupled between said first port, said second port, and said third port (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals), wherein the processor surrogate is characterized as not having its own central processing unit (Barker; Fig. 4, 202; [0026-0027]).;
- a third processing node coupled to said third port of said first processor surrogate in said second processing node (Fig. 1, processors 100 are connected to 4 adjacent actual processing nodes or pass-through processors);
- a fourth processing node coupled to said third processing node and to said first processing node (Fig. 1, processors 100 are connected to 4 adjacent actual processing nodes or pass-through processors); and
- a first input/output device coupled to said second port of said second processing node and accessible to said actual processor via said first processor surrogate (Kessler shows a

router/crossbar 200 that is responsible for appropriately forwarding communication signals to the I/O controller **104** and I/O devices **105 and 106**).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler and Barker.

For claim 29 Kessler in view of Barker teach:

The multiprocessor data processing system of claim 28 wherein said third processing node comprises a second processor surrogate (pass-through processor; col. 5, ll. 29-40; Fig. 1, processors 100 are connected to 4 adjacent actual processing nodes or pass-through processors) having a first port coupled to said third port of said first processor surrogate in said second processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), a second port (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]), a third port coupled to said fourth processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), and an interconnection circuit coupled between said first port, said second port, and said third port thereof (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler and Barker.

For claim 30 Kessler in view of Barker teach:

The multiprocessor data processing system of claim 29 further comprising:

- a second input/output device coupled to said second port of said second processor surrogate and accessible to said actual processor via said first processor surrogate and said second processor surrogate (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals to the I/O controller **104** and I/O devices **105 and 106**).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler and Barker.

For claim 31 Kessler in view of Barker teach:

The multiprocessor data processing system of claim 30 wherein said fourth processing node comprises a third processor surrogate (pass-through processor; col. 5, ll. 29-40; Fig. 1, processors 100 are connected to 4 adjacent actual processing nodes or pass-through processors) having a first port coupled to said third processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), a second port (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]), a third port coupled to said first processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), and an interconnection circuit coupled between said first port, said second port, and said third port thereof (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler and Barker.

For claim 32 Kessler in view of Barker teach:

The multiprocessor data processing system of claim 31 further comprising:

- a third input/output device coupled to said second port of said third processor surrogate and accessible to said actual processor via said third processor surrogate (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals to the I/O controller **104** and I/O devices **105 and 106**).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler and Barker.

12. Claims 7-8, 11, 17-18, and 25-26 rejected under 35 U.S.C. 103(a) as being unpatentable over Kessler in view of Barker as applied to claim 5, 9, 15, and 24 above, and further in view of the HyperTransport™ I/O Link Specification.

As discussed above, Kessler in view of Barker teach a multiprocessor system comprising a plurality of processing nodes **100**. Each processing node comprises a N, S, E, and W port for communicating with an adjacent processor (Fig. 1 and 2; col. 4, line 60 – col. 5, line 14). Furthermore, each processing node possesses a port for I/O communications (col. 5, ll. 15-20) and a port for memory communications (col. 5, ll. 21-28). Kessler goes on to teach, if a physical connection is not present between a pair of processors (i.e. a processor is missing or has been removed), a bypass path is implemented using a pass-through processor (col. 5, ll. 29-40). A pass-through processor permits each processor to access a pass-through processor's (a missing processor's) memory and I/O devices (col. 5, ll. 38-39). Kessler however fails to teach the communication link controller are substantially compatible with the HyperTransport™ I/O Link Specification.

The HyperTransport link is designed to deliver a high-performance and scalable interconnect between CPU, memory, and I/O devices. The HyperTransport link uses low swing differential signaling with on-die differential termination to achieve very high data rates. The HyperTransport link uses scalable frequency and data width to achieve scalable bandwidth.

HyperTransport technology provides significantly more bandwidth than current technologies, uses low-latency responses and low pin counts, and supports legacy PC buses. It is also designed to be extensible to new systems network architecture (SNA) buses, transparent to operating systems, and has little or no impact on peripheral drivers.

HyperTransport technology is designed for use in networking, telecommunications, computer, and high performance embedded applications, and any other application in which high speed, low latency, and scalability are necessary.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the HyperTransport communication protocol as the communication links of Kessler such that the multiprocessor system is provided with a high-speed, high-performance, point-to-point link for interconnecting integrated circuits.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

RMS

PAUL R. MYERS
PRIMARY EXAMINER